Gespac

BUS G-128

APPLICATION NOTE

DOUBLE EUROBOARD G-128 STANDARD BUS

Interconnection bus for 8/16/32 bit multiprocessor

Designed as a very powerful extension for the widely used G-64 bus, while retaining **full compatibility** with its predecessor, the G-128 bus concept is the optimum solution for double euroboard connection. The approach chosen by the designers offers all possible advantages:

- Indirect standard DIN 41612B connector, compatible with cable;
- **only** 2-row 64-pin instead of 3-row 96-pin, easier layout;
- parallel bus structure for multiprocessor arbitration;
- no need for a dedicated master processor unit;
- all I/O available in front of the board, no dedicated slot;
- no expensive front panel, can fit **into** standard rack;
- not dedicated to support only one microprocessor;
- optimum size 200 x 233,4 offers higher capability for top performance.

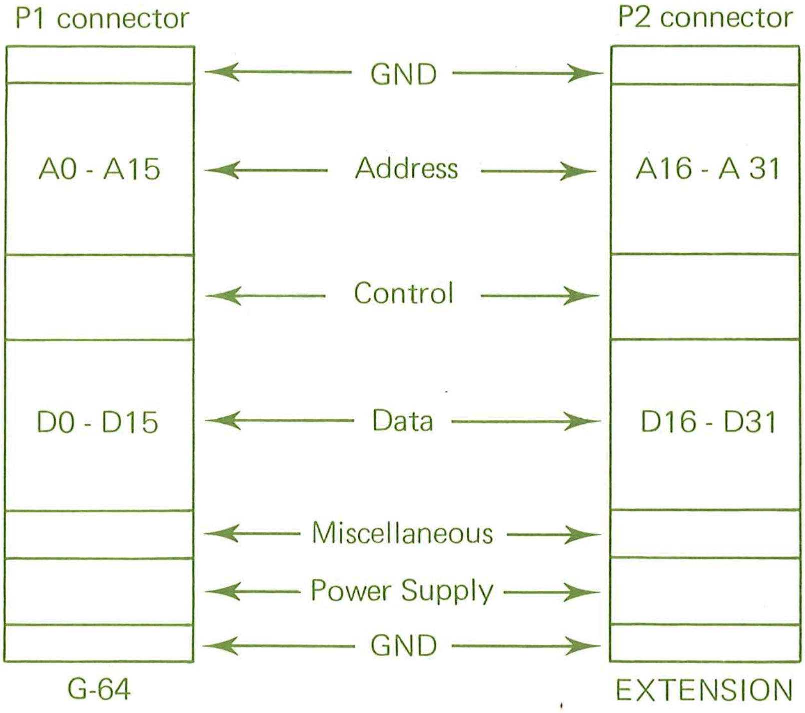
A lot of other reasons can show that the G-128 approach is very attractive for most designers. The basic advantage of the G-128 concept is its compatibility with the G-64 product line: having already an economical low end industrial product, the Gespac designers included all useful features in the high end data — processing line without any of the compromises necessary to cover both applications with only one type of boards.

Today the processor 68000 is available on G-128 euroboard. In 1982 the 16032 will also be introduced in this family of boards, and other processors will be included as soon as they become available and if there is a demand for them.

The bus itself is available in two sizes: 8 and 12 slot which allows to use the G-128 module in standard 15" rack with 8" or 5 1/4" floppy disk and winchester drive.

To recognise the product using the G-128 bus concept a symbol has been created with the same style as the G-64 logo:

G-128



G-128 Bus structure

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1. GENERAL INFORMATION

1.1 INTRODUCTION

The G-128 Bus is the powerful extension of the G-64 Bus, on a "double Europe" format. The G-128 Bus is compatible with the standard G-64 that is described in the application note AN0001E. Extension of the G-64 Bus consists essentially in adressing capability, word size, new concept in bus arbitration for multiprocessors philosophy and addition of new control lines.

1.2 FEATURES

The G-128 Bus provides the user with the following main features.

- 8 to 32 bit data transfers
- 32 address lines + 1 page signal
- Separate I/O select line (sync. 8 bit peripherals)
- 5 arbitration lines for bus request
- 1 arbitration clock
- Multiprocessors operations (up to 16 modules)
- Synchronous or asynchronous operation
- 8 interrupt levels
- 1 Parity error / Bus error control line
- 1 "System Fail" line
- Standard power supply lines ± 5Vdc and ± 12Vdc
- "Stand-by" power line (+ 5V batt.)

1.3 SPECIFICATIONS

Specifications for the G-128 Bus are identified in the table 1.1.

2. G-128 DESCRIPTION

2.1 G-128 CONNECTOR PIN DESCRIPTION

The signals name are identified in the table 2.1; for their definition and characteristics refer to table 2.2.

The G-128 Bus is realized with the G-64 Bus located on connector P1 and an extension on connector P2 as shown on fig. 2.2.

2.2 G-128 CONNECTORS

The G-128 Bus uses 2 standard DIN 41612-B female type connectors. G-128 modules use the corresponding male connectors. Mechanical dimensions for implementation are shown in fig. 2.1.

Power Requirements	+ 5Vdc + 5% – 3% + 12Vdc ± 5% – 12Vdc ± 5% – 5Vdc ± 5% + 5V batt: 3Vdc to + 5Vdc (option)
Interface	– Address: TTL compatible/high impedance – Data: TTL compatible/high impedance – Other signals: TTL compatible/open collector/high impedance
Address	32 lines + 1 "page" signal
Data transfers	8/16/32 bits
Bus connector	2 x 64 pin standard DIN 41612-B type connector
Signals polarity	– Logic: positive – Address: not inverted – Data: inverted – Control lines: all request signals are active at low level. All grant or acknowledge signals are active at high level except the lines that can be shared by several modules (or wired)
Master module driver characteristics	Low level output current IOL: 20 mA min High level output current IOH: –2 mA min
Loading rule on each module	1 TTL load max on each input: (I_{IL}: – 1,6 mA, I_{IH}: 40 μA)
Number of modules connected on the bus	16 modules max.
Module dimension	233.4 mm x 220 mm

Table 1.1 Specifications

P1 Connector (G-64)

ROW B		ROW A	
GND	1	GND	Power (2)
A8	2	A0	Address lines A0 to A15 (16)
A9	3	A1	
A10	4	A2	
A11	5	A3	
A12	6	A4	
A13	7	A5	
A14	8	A6	
A15	9	A7	
$\overline{\text{BRQ}}$	10	BGRT	Control lines (18)
$\overline{\text{RRQ}}$ ($\overline{\text{DS1}}$)	11	RGRT ($\overline{\text{DSO}}$)	
$\overline{\text{BGACK}}$	12	$\overline{\text{HALT}}$	
Enable	13	MCLK (SYCLK)	
$\overline{\text{RES}}$	14	$\overline{\text{VPA}}$	
$\overline{\text{NMI}}$ ($\overline{\text{INT7}}$)	15	RD$\overline{\text{Y}}$ ($\overline{\text{DTACK}}$)	
$\overline{\text{IRQ}}$ ($\overline{\text{INT2}}$)	16	$\overline{\text{VMA}}$ ($\overline{\text{AS}}$)	
$\overline{\text{FIRQ}}$ ($\overline{\text{INT6}}$)	17	R/$\overline{\text{W}}$	
IACK	18	Halt Ack	
$\overline{\text{D12}}$	19	$\overline{\text{D8}}$	DATA 2nd Byte (8)
$\overline{\text{D13}}$	20	$\overline{\text{D9}}$	
$\overline{\text{D14}}$	21	$\overline{\text{D10}}$	
$\overline{\text{D15}}$	22	$\overline{\text{D11}}$	
$\overline{\text{D4}}$	23	$\overline{\text{D0}}$	DATA 1st Byte (8)
$\overline{\text{D5}}$	24	$\overline{\text{D1}}$	
$\overline{\text{D6}}$	25	$\overline{\text{D2}}$	
$\overline{\text{D7}}$	26	$\overline{\text{D3}}$	
$\overline{\text{Parity error}}$ ($\overline{\text{BERR}}$)	27	$\overline{\text{Page}}$	Miscellaneous (4)
Chain In	28	Chain Out	
+ 5V Battery	29	– 5V	Power (8)
– 12V	30	+ 12V	
+ 5V	31	+ 5V	
GND	32	GND	

P2 Connector (G-128 extension)

ROW B		ROW A	
GND	1	GND	Power (2)
A24	2	A16	Address lines A16 to A31 (16)
A25	3	A17	
A26	4	A18	
A27	5	A19	
A28	6	A20	
A29	7	A21	
A30	8	A22	
A31	9	A23	
Reserved	10	Reserved	Control lines & Arbitration lines for bus request (18)
$\overline{\text{DS3}}$	11	$\overline{\text{DS2}}$	
$\overline{\text{BBUSY}}$	12	Reserved	
ARBCK	13	16 MHz Syst.	
$\overline{\text{INT 5}}$	14	$\overline{\text{P4}}$	
$\overline{\text{INT 4}}$	15	$\overline{\text{P3}}$	
$\overline{\text{INT 3}}$	16	$\overline{\text{P2}}$	
$\overline{\text{INT 1}}$	17	$\overline{\text{P1}}$	
$\overline{\text{INT 0}}$	18	$\overline{\text{P0}}$	
$\overline{\text{D28}}$	19	$\overline{\text{D24}}$	DATA 4th Byte (8)
$\overline{\text{D29}}$	20	$\overline{\text{D25}}$	
$\overline{\text{D30}}$	21	$\overline{\text{D26}}$	
$\overline{\text{D31}}$	22	$\overline{\text{D27}}$	
$\overline{\text{D20}}$	23	$\overline{\text{D16}}$	DATA 3rd Byte (8)
$\overline{\text{D21}}$	24	$\overline{\text{D17}}$	
$\overline{\text{D22}}$	25	$\overline{\text{D18}}$	
$\overline{\text{D23}}$	26	$\overline{\text{D19}}$	
$\overline{\text{SYSFAIL}}$	27	Reserved	Miscellaneous (4)
Reserved	28	Reserved	
+ 5V Battery	29	– 5V	Power (8)
– 12V	30	+ 12V	
+ 5V	31	+ 5V	
GND	32	GND	

Table 2.1 G-128 signals

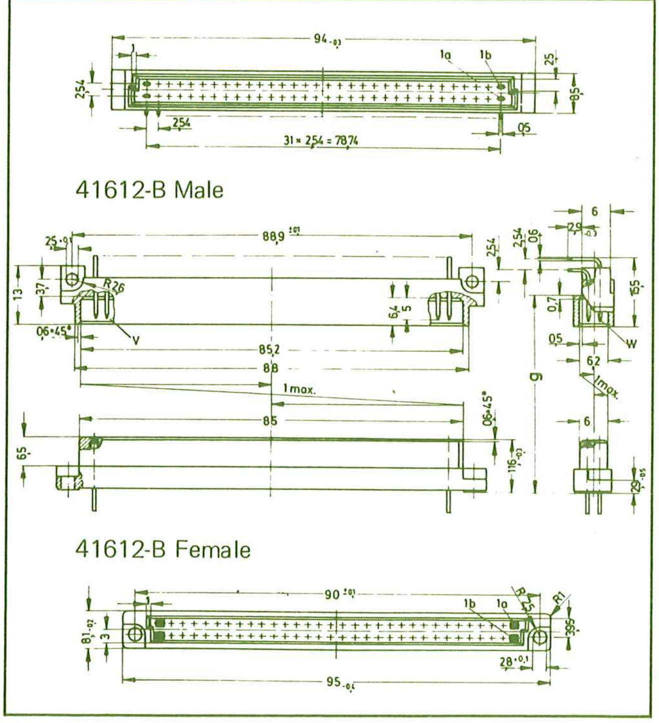


Fig. 2.1. Connector for G-128 standard

2.3 G-128 MODULES

G-128 modules are designed on the standard double "Europe" format shown in fig. 2.2.

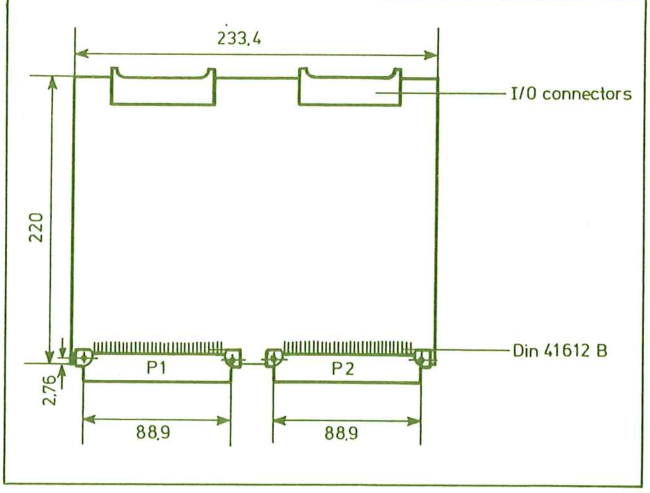


Fig. 2.2 Dimensions for G-128 modules

2.4 G-128 INTERFACE SIGNALS DEFINITION

Signals on P1 connector have been discussed in the G-64 application note (AN 0001 E), only extension signals of the G-128 will be defined here. Mnemomic, signal characteristics and pin number of P2 connector are identified in the table 2.2.

Nota:
- All input/output bus signal references are with respect to the current Bus Master
- Overlined terms are active or true when the voltage is low, other terms when the voltage is high.
- TS: "Three state" line
- T: "Totem pole" line
- O.C.: "Open collector" line

Table 2.2 P2 connector, A side. G-128 extension

Pin number	Signal mnemonic		Description
1a	GND		Ground – Power and signal ground.
2a-9a	A16-A23	TS	Address bus (bit 16-23)
10a	Reserved		Do not use
11a	$\overline{\text{DS2}}$	TS	Data Strobe 2 – Output signal to indicate a transfer of data D16-D23.
12a	Reserved		Do not use
13a	16 MHz Syst.		16 MHz System Clock. Reference 16 MHz clock output used for general timing.
14a-18a	$\overline{\text{P4}}$-$\overline{\text{P0}}$	O.C.	Priority Bus Request – These signals in conjunction with the ARBCK signal allow a distributed bus arbitration.
19a-22a	$\overline{\text{D24}}$-$\overline{\text{D27}}$	TS	Data Bus (bit 24-27) – Bidirectional data lines used for data transfer between the bus master and all other modules.
23a-26a	$\overline{\text{D16}}$-$\overline{\text{D19}}$	TS	Data Bus (bit 16-19) – Same as pin 19a
27a	Reserved		Do not use
28a	Reserved		Do not use
29a	– 5V		– 5Vdc power supply
30a	+ 12V		+ 12Vdc power supply
31a	+ 5V		+ 5Vdc power supply
32a	GND		Ground – Same as pin 1a

Table 2.2 P2 connector, B side. G-128 extension

1b	GND		Ground – Same as pin 1a
2b-9b	A24-A31	TS	Address Bus (bit 24-31)
10b	Reserved		Do not use
11b	$\overline{\text{DS3}}$	TS	Data Strobe 3 – Output signal to indicate a transfer of data D24-D31.
12b	$\overline{\text{BBUSY}}$	O.C.	Bus Busy – Output signal generated by the current bus master to indicate that it is using the bus in multiprocessors operations.
13b	ARBCK	T	Arbitration clock – Clock used in conjunction with P0-P3 signals for a distributed bus arbitration.
14b	$\overline{\text{INT5}}$	O.C.	Interrupt Request 5 – Input signal that generates a priority interrupt. Level 7 is the highest priority.
15b	$\overline{\text{INT4}}$	O.C.	Interrupt Request 4 – Same as pin 14b
16b	$\overline{\text{INT3}}$	O.C.	Interrupt Request 3 – Same as pin 14b

17b	$\overline{\text{INT1}}$	O.C.	Interrupt Request 1 — Same as pin 14b
18b	$\overline{\text{INT0}}$	O.C.	Interrupt Request 0 — Same as pin 14b
19b-22b	$\overline{\text{D28}}$-$\overline{\text{D31}}$	TS	Data Bus (bit 28-31) — Same as pin 19a
23b-26b	$\overline{\text{D20}}$-$\overline{\text{D23}}$	TS	Data Bus (bit 20-23) — Same as pin 19a
27b	$\overline{\text{SYSFAIL}}$	O.C.	System Fail — Bidirectional signal that is active when a module is not (or not yet) operational in the system.
28b	Reserved		Do not use
29b	+ 5VBAT		+ 5Vdc Battery — Line used to supply modules requiring battery backup.
30b	— 12V		— 12Vdc power supply
31b	+ 5V		+ 5Vdc power supply — Same as pin 31a
32b	GND		Ground — Same as pin 1a

3. SYNCHRONOUS/ASYNCHRONOUS READ OR WRITE OPERATION

3.1 INTRODUCTION

Timing for read or write operation has been discussed in the G-64 Bus application note (AN 0001 E) and it applies directly to the G-128 standard.

3.2 GENERAL INFORMATION

Dynamic characteristics that will be defined correspond to the G-128 bus signals. Symbols used are shown on fig. 3.1.

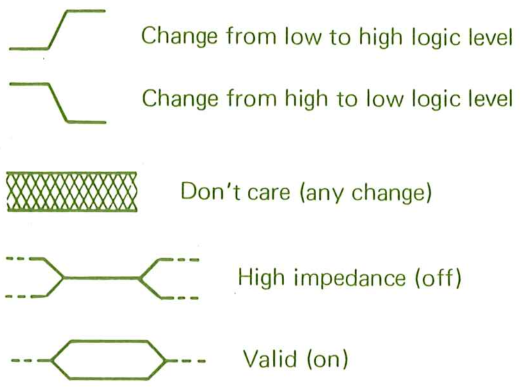

Change from low to high logic level
Change from high to low logic level
Don't care (any change)
High impedance (off)
Valid (on)

Fig. 3.1 Signal symbols

3.3 SYNCHRONOUS READ-WRITE OPERATION

All transfers are synchronous with ENABLE signal and controlled by R/W, VMA (or VPA) signals, as shown on fig. 3.2. Timing values are given in table 3.1.

Ready signal allows slow memory or peripheral connection on the G-128 bus. Ready signal is considered as an asynchronous signal. Its timing is shown in fig. 3.2.

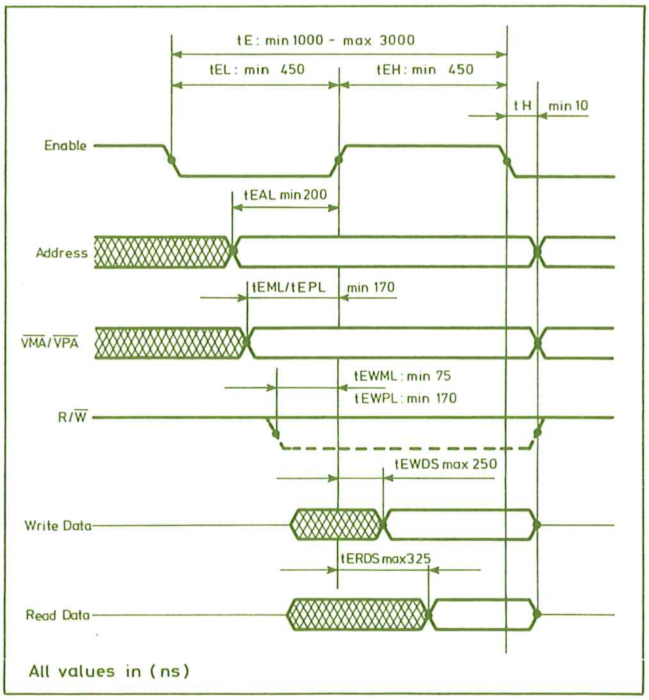


Fig. 3.2 Synchronous Read/Write timing

Signal name	Description	Value (ns)	
		Min	Max
tE	Cycle time	1000	3000
tEL	Pulse width low	450	
tEH	Pulse width high	450	
tEAL	Address lead time for memory	200	
tEML	VMA command lead time	170	
tEPL	VPA command lead time	170	
tEWML	Write lead time for memory	75	
tEWPL	Write lead time for peripheral	170	
tEWDS	Data set-up time for write cycle		250
tERDS	Data set-up time for read cycle		325
tH	Hold time	10	

Table 3.1 Synchronous Read/Write timing

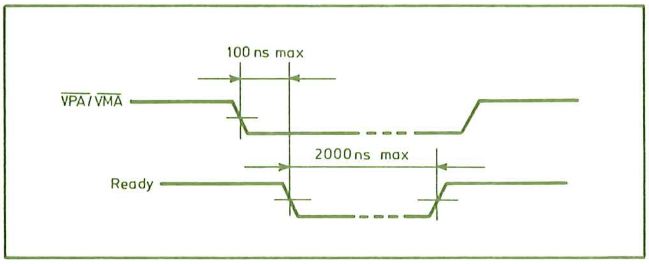


Fig. 3.2 Ready control

3.4 ASYNCHRONOUS READ/WRITE OPERATION

The G-128 bus is intended to perform 16/32 bit asynchronous operations by supporting microprocessor modules as performant as the GESMPU-D1 using the 68000 microprocessor.

Peripheral modules working in a synchronous mode can still be used and share the same bus with asynchronous modules. However, a synchronous cycle will be generated each time that a synchronous module is addressed.

An asynchronous read sequence is shown fig. 3.3 and a write sequence on fig. 3.4. Refer to the diagram of fig. 3.5 and table 3.2 for the timing.

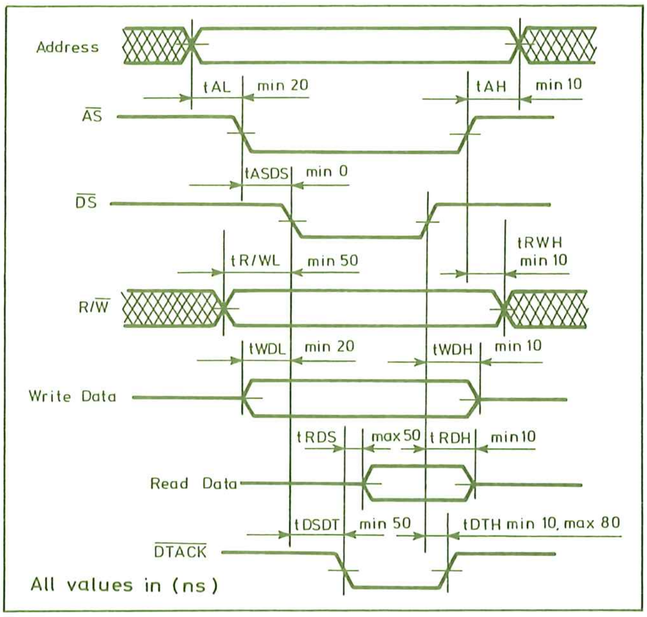
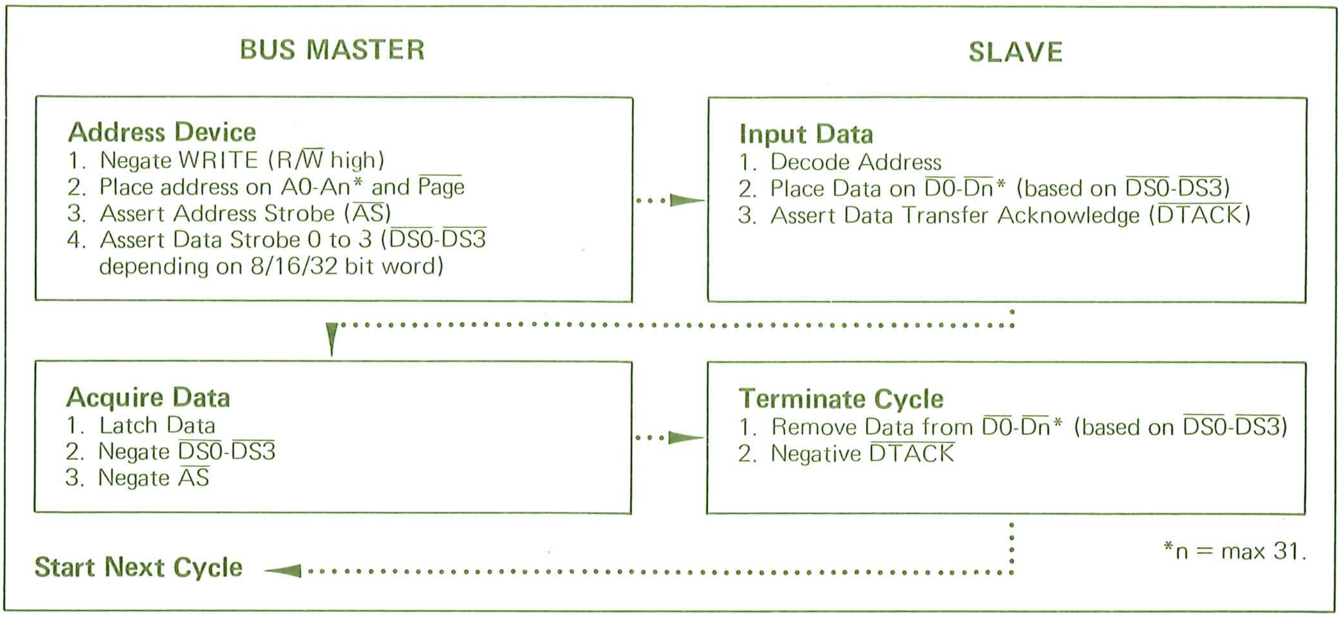


Fig. 3.5 Read-Write Timing



BUS MASTER

SLAVE

Address Device
1. Negate WRITE (R/$\overline{W}$ high)
2. Place address on A0-An* and $\overline{Page}$
3. Assert Address Strobe ($\overline{AS}$)
4. Assert Data Strobe 0 to 3 ($\overline{DS0}$-$\overline{DS3}$ depending on 8/16/32 bit word)

Input Data
1. Decode Address
2. Place Data on $\overline{D0}$-$\overline{Dn}$* (based on $\overline{DS0}$-$\overline{DS3}$)
3. Assert Data Transfer Acknowledge ($\overline{DTACK}$)

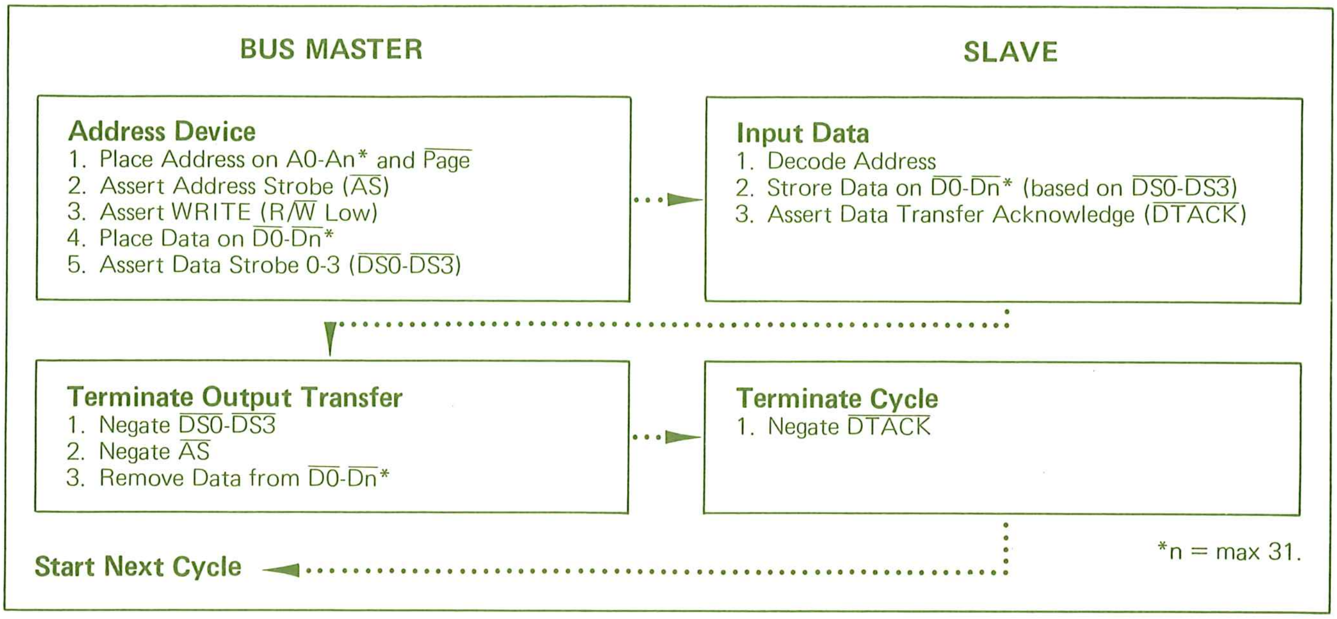
Acquire Data
1. Latch Data
2. Negate $\overline{DS0}$-DS3
3. Negate $\overline{AS}$

Terminate Cycle
1. Remove Data from $\overline{D0}$-$\overline{Dn}$* (based on $\overline{DS0}$-$\overline{DS3}$)
2. Negative $\overline{DTACK}$

Start Next Cycle

*n = max 31.

Fig. 3.3 Asynchronous Read sequence



BUS MASTER

SLAVE

Address Device
1. Place Address on A0-An* and $\overline{\text{Page}}$
2. Assert Address Strobe ($\overline{\text{AS}}$)
3. Assert WRITE (R/$\overline{\text{W}}$ Low)
4. Place Data on $\overline{\text{D0}}$-$\overline{\text{Dn}}$*
5. Assert Data Strobe 0-3 ($\overline{\text{DS0}}$-$\overline{\text{DS3}}$)

Input Data
1. Decode Address
2. Strore Data on $\overline{\text{D0}}$-$\overline{\text{Dn}}$* (based on $\overline{\text{DS0}}$-$\overline{\text{DS3}}$)
3. Assert Data Transfer Acknowledge ($\overline{\text{DTACK}}$)

Terminate Output Transfer
1. Negate $\overline{\text{DS0}}$-$\overline{\text{DS3}}$
2. Negate $\overline{\text{AS}}$
3. Remove Data from $\overline{\text{D0}}$-$\overline{\text{Dn}}$*

Terminate Cycle
1. Negate $\overline{\text{DTACK}}$

Start Next Cycle

*n = max 31.

Fig. 3.4 Asynchronous Write sequence

Signal name	Description	Value (ns)	
		min	max
tAL	Adress Lead Time	20	
tASDS	Address strobe to data strobe delay	0	
tRWL	Read or write command lead time	50	
tWDL	Write data lead time	20	
tWDH	Write data hold time	10	
tDSDT	Data strobe to data acknowledge	50	*
tDTH	Data acknowledge command hold time	10	80
tRDS	Read data set up time		50
tRDH	Read data hold time	10	
tAH	Address hold time	10	
tRWH	Read or write command hold time	10	

Table 3.2 G-128 Bus Asynchronous Timing

* Asynchronous data transfer allows tDSDT to be as long as required by the selected device but data transfer has to be supervised by a timer to avoid waiting for a non responding device. If a transfer is too long, the timer will generate a Bus error (BERR) signal. Thus tDSDT must be shorter than the timer period. Fig. 3.6 illustrates the "BERR" timing.

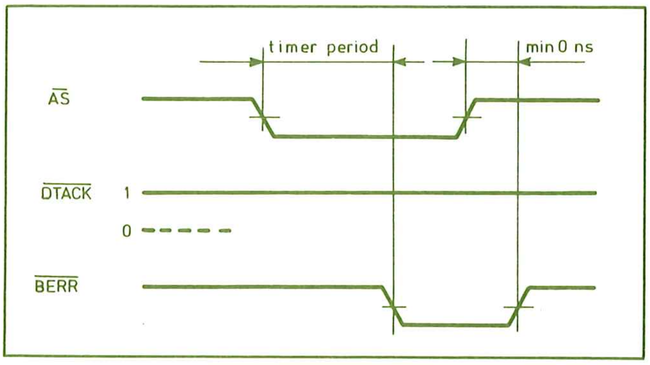


Fig. 3.6 Bus error timing

4. G-128 BUS ARBITRATION

4.1 INTRODUCTION

In the G-128 standard, bus arbitration principle has been elaborated in order to facilitate multiprocessors systems design without the need of a sophisticated central bus arbitrator but rather by a distributed bus arbitration philosophy.

4.2 G-128 BUS ARBITRATION SIGNALS

The Bus arbitration needs the use of the following signals which are identified in tables 2.1 and 2.2:

ARBCK	Arbitration clock
$\overline{\text{BBUSY}}$*	Bus busy
$\overline{\text{P0}}$*-$\overline{\text{P3}}$*	Priority bus request 0-3
$\overline{\text{P4}}$*	Priority bus request 4 (Reserved)

*Open collector

These signals allow a distributed bus arbitration. Each possible Bus Master (processor or DMA global device) must compete for the bus by putting its address/priority on the $\overline{\text{P0}}$-$\overline{\text{P4}}$ lines. $\overline{\text{P4}}$ is the highest priority address bit and may be used for emergency bus requests. $\overline{\text{P4}}$ must be software programmable while address on $\overline{\text{P0}}$-$\overline{\text{P3}}$ lines may be set by hardware. In this way the arbitration network allows 16 Bus Requesters to share the same backplane. Arbitration is controlled by the ARBCK clock and $\overline{\text{BBUSY}}$ signal.

4.3 ARBITRATION PRINCIPLE

Each Bus Requester puts its address/priority on $\overline{\text{P0}}$-$\overline{\text{P4}}$ lines at the raising edge of the arbitration clock. At the falling edge of the clock, only 1 competing master can recognize its address/priority stabilized on the bus. At the next raising edge of the clock, this master takes the bus mastership by asserting $\overline{\text{BBUSY}}$ (if this signal is not asserted!) and the next arbitration cycle starts.

The current bus master can keep the bus as long as it wants by maintaining the $\overline{\text{BBUSY}}$ line asserted, but by monitoring the arbitration, it should release the bus when it sees that it has lost the bus contention.

The bus mastership must be released at a falling edge of the arbitration clock.

4.4 ARBITRATION TIMING

Arbitration signals are shown on fig. 4.1, timing values are given in the table 4.1.

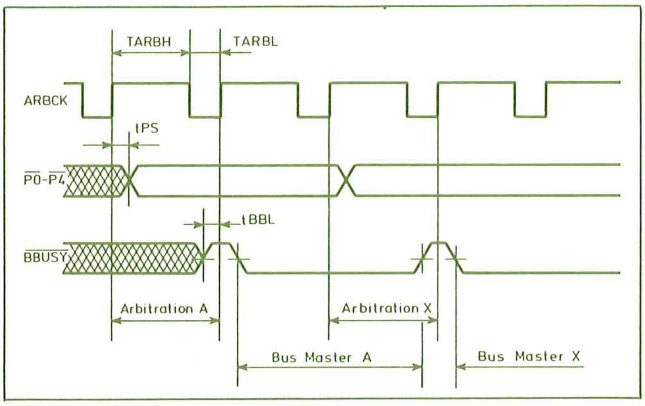


Fig 4.1 Arbitration timing

Signal name	Description	Value (ns)	
		min	max
tARBH	Pulse width high		
tARBL	Pulse width Low		
tPS	P0-P4 set up time		50
tBBL	Bus busy lead time	20	

Table 4.1 Arbitration timing values

5. INTERRUPTS

The G-128 Bus provides the user with 8 interrupt lines, $\overline{\text{INT0}}$-$\overline{\text{INT7}}$. Peripheral devices (or processors) can request an interrupt by asserting one of these lines.

Each processor module has an on-board interrupt controller which generates local interrupt vectors. The desired interrupt lines can be connected to the interrupt controller inputs by jumpers on the board.

Falling edges on $\overline{\text{INT0}}$-$\overline{\text{INT7}}$ lines will create interrupts for all connected processor boards. There is no interrupt acknowledge cycle on the bus, so the interrupt devices should clear their requests by themselves (or by software).

If several devices do use the same INT line, a polling software process is necessary in order to identify the interrupting device(s).

6. MISCELLANEOUS

6.1 SYSTEM FAILURE

The system modules able to test themselves will perform self-check processes (at power-up or system reset in particular). They should assert the $\overline{\text{SYSFAIL}}$ line as long as they are not operational.

6.2 BACKPLANE

Pull-up resistors should be mounted on the backplane at the end of the bus open collector lines.

WARNING:
This is a preliminary specification; all characteristics are subject to change without notice.

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